47. (New) The integrated circuit structure of claim 46, wherein the first plurality of doped regions and the second plurality of doped regions are arranged in a rectangular array.

48. (New) The integrated circuit structure of claim 46, wherein the gate region is a unitary gate structure separating adjacent doped regions of the first plurality of doped regions and the second plurality of doped regions.

49. (New) The integrated circuit structure of claim 46, wherein the first plurality of doped regions and the second plurality of doped regions are substantially rectangular, and the gate region forms a rectangular grid separating the first plurality of doped regions and the second plurality of doped regions.

50. (New) The integrated circuit structure of claim 46, wherein the first plurality of doped regions are source regions of a distributed transistor array and the second plurality of doped regions are drain regions of the distributed transistor array.

51. (New) The integrated circuit structure of claim 50, wherein the distributed transistor array operates as a switch in a switching regulator circuit.

52. (New) The integrated circuit structure of claim 50, wherein the distributed transistor array is a PMOS transistor.

53. (New) The integrated circuit structure of claim 50, wherein the distributed transistor array is an NMOS transistor.

54. (New) A voltage regulator having an input terminal and an output terminal, comprising:

a printed circuit board;

a first flip-chip type integrated circuit chip mounted on the printed circuit board, the first integrated circuit chip including a first power switch fabricated therein to alternately couple and decouple the input terminal to the output terminal, wherein the power switch includes

a chip substrate having a first plurality of doped regions and a second plurality of doped regions, the first plurality of doped regions and the second plurality of doped regions being arranged in an alternating pattern, the first plurality of doped regions coupled to the input terminal, the second plurality of doped regions coupled to the output terminal, and

a gate region on the chip substrate separating the first plurality of doped regions and the second plurality of doped regions;

a filter disposed to provide a substantially DC voltage at the output terminal; and

a control circuit connected to the gate region to control the power switch to maintain the DC voltage substantially constant.

10 9
~~58~~. (New) The voltage regulator of claim ~~54~~, wherein the first plurality of doped regions and the second plurality of doped regions are arranged in a rectangular array.

11 9
~~56~~. (New) The voltage regulator of claim ~~54~~, wherein the gate region is a unitary gate structure separating adjacent doped regions of the first plurality of doped regions and the second plurality of doped regions.

12 9
~~57~~. (New) The voltage regulator of claim ~~54~~, wherein the first plurality of doped regions and the second plurality of doped regions are substantially rectangular, and the gate region forms a rectangular grid separating the first plurality of doped regions and the second plurality of doped regions.

13 9
~~58~~. (New) The voltage regulator of claim ~~54~~, wherein the first plurality of doped regions are source regions of a distributed transistor array and the second plurality of doped regions are drain regions of the distributed transistor array.

14 13
~~59~~. (New) The voltage regulator of claim ~~58~~, wherein the distributed transistor array is a PMOS transistor.

15 13
~~60~~. (New) The voltage regulator of claim ~~58~~, wherein the distributed transistor array is an NMOS transistor.

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61. (New) The voltage regulator of claim 54, wherein the first power switch and filter form a buck-converter topology.

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62. (New) The voltage regulator of claim 54, wherein the first power switch intermittently couples an intermediate terminal to the input terminal.

18 17
63. (New) The voltage regulator of claim 62, wherein the first flip-chip type integrated circuit chip has a second power switch fabricated therein to alternately couple and decouple the intermediate terminal to ground.

19 18
64. (New) The voltage regulator of claim 63, wherein the filter is electrically coupled between the output terminal and the intermediate terminal.

20 18
65. (New) The voltage regulator of claim 63, wherein the first power switch includes a distributed array of PMOS transistors and the second power switch includes a distributed array of NMOS transistors.

21 17
66. (New) The voltage regulator of claim 62, further comprising a rectifier connecting the intermediate terminal to ground.

22
67. (New) An integrated circuit chip with a power switch for a voltage regulator fabricated thereon, comprising:

a substrate having a first plurality of doped regions and a second plurality of doped regions, the first plurality of doped regions and the second plurality of doped regions being arranged in a first alternating pattern;

a gate region on the substrate separating the first plurality of doped regions and the second plurality of doped regions; and

an array of metalized pads fabricated on a surface of the substrate, the array including a first plurality of pads and a second plurality of pads, the first and second pluralities of pads being arranged in a second alternating pattern;

wherein the first plurality of pads are electrically connected to the first plurality of doped regions and the second plurality of pads are electrically connected to the second plurality of

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doped regions, and wherein the first plurality of pads are connected to a first terminal of the voltage regulator and the second plurality of pads are connected to a second terminal in the voltage regulator.

23 22
68. (New) The chip of claim 67, wherein the first alternating pattern is a rectangular array.

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69. (New) The chip of claim 67, wherein the gate region is a unitary gate structure separating adjacent doped regions of the first plurality of doped regions and the second plurality of doped regions.

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70. (New) The chip of claim 67, wherein the first plurality of doped regions and the second plurality of doped regions are substantially rectangular, and the gate region forms a rectangular grid separating the first plurality of doped regions and the second plurality of doped regions.

24 22
71. (New) The chip of claim 67, wherein the first plurality of doped regions are source regions of a distributed transistor array and the second plurality of doped regions are drain regions of the distributed transistor array.

27 26
72. (New) The chip of claim 71, wherein the distributed transistor array operates as a switch in a switching regulator circuit.

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73. (New) The chip of claim 67, wherein the second alternating pattern is a first set of alternating stripes.

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74. (New) The chip of claim 67, wherein the second alternating pattern is a checkerboard pattern.

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75. (New) The chip of claim 67, wherein the first and second pluralities of doped regions are p+ regions formed in an n-type well or substrate.

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